CLAIMS

1. A radiation detector assembly, comprising:

a semiconductor detector array substrate, comprising CdZnTe or CdTe, having a plurality of detector cell pads on a first surface thereof said pads comprising a contact metallization and a solder barrier metallization

an interposer card having planar dimensions no larger than planar dimensions of the semiconductor detector array substrate

a plurality of interconnect pads on a first surface thereof,

at least one readout semiconductor chip and at least one connector on a second surface thereof

each having planar dimensions no larger than the planar dimensions of the interposer card

solder columns that extend from contacts on the interposer first surface to the plurality of pads on the semiconductor detector array substrate first surface

said solder columns comprising at least one solder having a melting point or liquidus less than 120 degrees C

an encapsulant between said interposer circuit card first surface and the semiconductor detector array substrate first surface, encapsulating said solder columns

said encapsulant curing at a temperature no greater than 120 degrees C.

2. The assembly of claim 1 wherein said encapsulant comprises a cured polymer fluxing agent.

3. The assembly of claim 1 wherein said contact metallization comprises a layer of one selected from the list that includes Pt, Au, Al, Ni, Pd, and Ti.

4. The assembly of claim 1 wherein said barrier metallization comprises one or more layers of metals selected from the list that includes Ni, Au, Ti, V, and Cu.

5. A method for making a detector array assembly that comprises the steps of:

providing a semiconductor detector array substrate comprising CdZnTe or CdTe having a plurality of metallized detector cell pads on a first surface thereof, said pads comprising a contact metallization and a solder barrier metallization on a first surface thereof

providing an interposer card having

planar dimensions no larger than the planar dimensions of the semiconductor detector array substrate

at least one readout semiconductor chip on a second surface thereof, and

at least one connector on a second surface thereof,

each of planar dimensions no larger than the planar dimensions of the interposer card

a plurality of discrete solder bumps on a first surface thereof at least one bump corresponding to at least one pad on said semiconductor detector array substrate,

disposing a fluxing agent between the interposer card and the semiconductor detector array substrate; and

mating the interposer card first surface to the semiconductor detector array substrate first surface, wherein the solder bumps face towards and are aligned with their corresponding pads, such that there exists fluxing agent at least between said bumps said detector substrate pads

heating the combined unit to a temperature not exceeding 120 degrees C, allowing sufficient time for at least a portion of the solder to melt and bond to the detector substrate

cooling to allow the solder to harden.

6. The method of claim 5 wherein said solder bumps comprise a solder with a melting point or liquidus less than 120 degrees C

7. The method of claim 5 wherein said metallized detector cell pads further comprise a solder with a melting point or liquidus less than 120 degrees C

8. The method of claim 5 wherein, after cooling, a liquid encapsulant is introduced between the two first surfaces and cured a temperature no greater than 120 degrees C

9. The method of claim 5 wherein said fluxing agent further comprises a polymer encapsulant that cures at a temperature no greater than 120 degrees C

10. The method of claim 9 wherein heating of the said combined unit and encapsulant continues until said encapsulant is fully hardened.

11. The method of claim 9 wherein heating of the said combined unit melts the solder and simultaneously hardens the encapsulant.

12. The method of claim 9 wherein heating of the said combined unit and encapsulant proceeds until said encapsulant is fully hardened.

13. The method of claim 5 wherein said contact metallization comprises a layer of one selected from the list that includes Pt, Au, Al, Ni, Pd, and Ti.

14. The method of claim 5 wherein said barrier metallization comprises one or more layers of metals selected from the list that includes Ni, Au, Ti, V, and Cu.

15. The method of claim 5 wherein said cell pads metallization further comprises a solder having a melting point or liquidus below 120 degrees C.

16. The method of claim 5 wherein said cell pads metallization further comprises a solder having a melting point or liquidus below 120 degrees C.

17. The method of claim 5 wherein said solder bumps further comprises a solder having a melting point or liquidus below 120 degrees C.